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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,819	04/08/2004	Philip D. Cole	010327-005820US	9057

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,819	COLE, PHILIP D.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 8 April 2004. These drawings are deemed acceptable for examination.

Specification

2. The abstract of the disclosure is objected to because of the following:

All extraneous markings, such as "Attorney Docket ..." should be removed from the abstract.

The word "writes" in line 6 of the abstract should be changed to "writing".

Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

Examiner respectfully requests that Applicant add a reference to the parent application (10/160,664), and corresponding issued patent (6,721,229) to the first page of the specification

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, Applicant fails to disclose the first and third sets of SDRAM banks as sharing a common SDRAM bank.

Double Patenting

5. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

6. A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. Claims 1-8 and 13-22 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-4, 7, 6, 5 and 8-18 respectively, of prior U.S. Patent No. 6,721,229. This is a double patenting rejection.

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

9. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

10. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 9-12 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,721,229 (hereinafter US Patent '229) in view of Nunziata (US Patent 5,619,471).

As for claim 9, all of the limitations of this claim are explicitly taught in claim 1 of US Patent '229, hence US Patent '229 anticipates claim 9 of the instant application.

As for claims 10-11, though claim 1 of US Patent '229 teaches all the limitations of claim 9, it fails to set forth a third and forth set of SDRAM banks as being read in an interleaved fashion. Additionally, US Patent '229 fails to teach each set of SDRAM banks as including at least two SDRAM banks.

Nunziata however teaches reading data using a third set of SDRAM banks (Fig. 2, bank 2), and reading data using a fourth set of SDRAM banks, wherein the third set of SDRAM banks and the fourth set of SDRAM banks write interleaved (Fig. 2, bank 3 comprises the fourth set - col. 4, lines 35-59, the memory controller (Fig. 2, element 20) can read or write to each of the four memory banks in an interleaved fashion (i.e. alternating banks within the interleaved pair)). Additionally, though Nunziata describes four "banks", each bank as disclosed in Fig. 2 actually comprises a set of multiple banks of DRAM (referring to Fig. 4, each "bank" comprises four unique banks comprising two DRAM each. Hence each "bank" as described in Fig. 2, is actually a set of banks as claimed by Applicant).

As for claim 12, US Patent '229 fails to teach the first and third set of SDRAM banks as sharing a common SDRAM bus, however Nunziata teaches a plurality of registers (Fig. 2, element 44) which are used to maintain information relating to each of

the four memory banks. This register is coupled to all four banks, as it is part of the controller, which is used to control access to each of the four banks. One of the registers in particular (as disclosed in Fig. 8a), comprises information that is common to all four of the memory banks. The register itself is shared among the four banks as the controller uses this register in particular to access information relevant to all of the banks (col. 10, lines 1-13). Though the register is not explicitly taught as being an SDRAM bank, it would have been obvious to one of ordinary skill in the art at the time of the invention for Nunziata to use an SDRAM bank for this register to decrease the access time of data stored within the register.

It would have been obvious to one of ordinary skill in the art at time of the invention for the teachings disclosed by US Patent '229 to further include Nunziata's memory controller for both interleaved and non-interleaved memory. By doing so, US Patent '229 would have a means of further increasing the access speed of the memory, by making use of Nunziata's interleaving scheme as described in col. 2, lines 1-14.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nunziata.

As for claims 9-10, Nunziata teaches a method of transmitting data using synchronous dynamic random access memory (SDRAM), the method comprising:

writing data using a first set of SDRAM banks (Fig. 2, bank 0);

writing data using a second set of SDRAM banks, wherein the first set of SDRAM banks and the second set of SDRAM banks write interleaved (Fig. 2, bank 1 comprises the second set – col. 4, lines 35-59, the memory controller (Fig. 2, element 20) can read or write to each of the four memory banks in an interleaved fashion (i.e. alternating banks within the interleaved pair));

reading data using a third set of SDRAM banks (Fig. 2, bank 2); and

reading data using a fourth set of SDRAM banks, wherein the third set of SDRAM banks and the fourth set of SDRAM banks write interleaved (Fig. 2, bank 3 comprises the fourth set - col. 4, lines 35-59, the memory controller (Fig. 2, element 20) can read or write to each of the four memory banks in an interleaved fashion (i.e. alternating banks within the interleaved pair)).

It is worthy to note that though Nunziata describes four "banks", each bank as disclosed in Fig. 2 actually comprises a set of multiple banks of DRAM (referring to Fig. 4, each "bank" comprises four unique banks comprising two DRAM each. Hence each "bank" as described in Fig. 2, is actually a set of banks as claimed by Applicant.

Additionally, though Nunziata teaches DRAM, she fails to explicitly teach SDRAM, however using SDRAM in place of DRAM would have been obvious to one of ordinary skill in the art at the time of the invention in order to exploit the well-known benefits of SDRAM. Numerous benefits are commonly understood in the art, such as an increased access speed in comparison to convention DRAM memory.

As for claim 11, Nunziata teaches each set of SDRAM banks as including at least two SDRAM banks (Nunziata describes four "banks", each bank as disclosed in Fig. 2 actually comprises a set of multiple banks of DRAM (referring to Fig. 4, each "bank" comprises four unique banks comprising two DRAM each).

As for claim 12, Nunziata teaches the first set of DRAM banks and third set of DRAM banks as sharing a common SDRAM bank. As understood, the "broadest reasonable interpretation consistent with [Applicant's] specification" given to this limitation includes an SDRAM bank that is common to both said first and said third SDRAM bank, and shared by both of the first and third banks. Nunziata teaches a plurality of registers (Fig. 2, element 44) which are used to maintain information relating to each of the four memory banks. This register is coupled to all four banks, as it is part of the controller, which is used to control access to each of the four banks. One of the registers in particular (as disclosed in Fig. 8a), comprises information that is common to all four of the memory banks. The register itself is shared among the four banks as the controller using this register in particular to access information relevant to all of the banks (col.

10, lines 1-13). Though the register is not explicitly taught as being an SDRAM bank, it would have been obvious to one of ordinary skill in the art at the time of the invention for Nunziata to use an SDRAM bank for this register to decrease the access time of data stored within the register.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Estakhri et al. (US Patent 6,397,314 B1) teach increasing the memory performance of flash memory devices by writing sectors simultaneously to multiple flash memory devices.

Burroughs et al. (US Patent 6,076,136) teach a RAM address decoding system and method to support misaligned memory access.

Stracovsky et al. (US Patent 6,286,075 B1) teach a method for speeding up access to a memory page.

Schulz et al. (US PG Publication 2003/0046501 A1) teach a method for interleaving memory.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

5/5/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER